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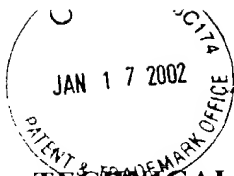
**Capacitors, DRAM Arrays, Monolithic Integrated
Circuits, And Methods Of Forming Capacitors,
DRAM Arrays, And Monolithic Integrated Circuits**

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TECHNICAL FIELD

The invention pertains to semiconductor capacitor constructions and to methods of forming semiconductor capacitor constructions. The invention is thought to have particular significance in application to methods of forming dynamic random access memory (DRAM) cell structures, to DRAM cell structures, and to integrated circuitry incorporating DRAM cell structures.

BACKGROUND OF THE INVENTION

A commonly used semiconductor memory device is a DRAM cell. A DRAM cell generally consists of a capacitor coupled through a transistor to a bitline. A semiconductor wafer fragment 10 is illustrated in Fig. 1 showing a prior art DRAM array 83. Wafer fragment 10 comprises a semiconductive material 12, field oxide regions 14, and wordlines 24 and 26. Wordlines 24 and 26 comprise a gate oxide layer 16, a polysilicon layer 18, a silicide layer 20 and a silicon oxide layer 22. Silicide layer 20 comprises a refractory metal silicide, such as tungsten silicide, and polysilicon layer 18 typically comprises polysilicon doped with a conductivity enhancing dopant. Nitride spacers 30 are laterally adjacent wordlines 24 and 26.

Electrical node locations 25, 27 and 29 are between wordlines 24 and 26 and are electrically connected by transistor gates comprised by wordlines 24 and 26. Node locations 25, 27 and 29 are diffusion regions formed within semiconductive material 12.

A borophosphosilicate glass (BPSG) layer 34 is over semiconductive material 12 and wordlines 24 and 26. An oxide layer 32 is provided

1 between BPSG layer 34 and material 12. Oxide layer 32 inhibits diffusion
2 of phosphorus from BPSG layer 34 into underlying materials.

3 Conductive pedestals 54, 55 and 56 extend through BPSG layer 34 to
4 node locations 25, 27 and 29, respectively. Capacitor constructions 62 and
5 64 contact upper surfaces of pedestals 54 and 56, respectively. Capacitor
6 constructions 62 and 64 comprise a storage node layer 66, a dielectric layer
7 68, and a cell plate layer 70. Dielectric layer 68 comprises an electrically
8 insulative layer, such as silicon nitride. Cell plate layer 70 comprises
9 conductively doped polysilicon, and may alternatively be referred to as a cell
10 layer 70. Storage node layer 66 comprises conductively doped hemispherical
11 grain (HSG) polysilicon.

12 A conductive bitline plug 75 contacts an upper surface of pedestal 55.
13 Bitline plug 75 may comprise, for example, tungsten. Together, bitline plug
14 75 and pedestal 55 comprise a bitline contact 77.

15 A bitline 76 extends over capacitors 62 and 64 and in electrical
16 connection with bitline contact 77. Bitline 76 may comprise, for example,
17 aluminum.

18 The capacitors 62 and 64 are electrically connected to bitline contact
19 77 through transistor gates comprised by wordlines 26. A first DRAM cell
20 79 comprises capacitor 62 electrically connected to bitline 76 through a
21 wordline 26 and bitline contact 77. A second DRAM cell 81 comprises
22 capacitor 64 electrically connected to bitline 76 through wordline a 26 and
23 bitline contact 77. DRAM array 83 comprises first and second DRAM
24 cells 79 and 81.

1 If capacitors 62 and 64 are inadvertently shorted together, a so-called
2 "double bit failure" will occur. Such double bit failures can occur if a stray
3 piece of polysilicon, or HSG polysilicon, breaks off during formation of
4 DRAM array 83 and disadvantageously electrically connects capacitors 62 and
5 64. Prior art capacitor fabrication methods employ chemical-mechanical
6 polishing (CMP) of HSG polysilicon. HSG polysilicon pieces can break off
7 during such CMP processes and cause double bit failures. It would be
8 desirable to develop alternative DRAM constructions which could be formed
9 by methods avoiding double bit failures.

10 11 SUMMARY OF THE INVENTION

12 The invention includes a number of methods and structures pertaining
13 to semiconductor circuit technology, including: methods of forming DRAM
14 memory cell constructions; methods of forming capacitor constructions; DRAM
15 memory cell constructions; capacitor constructions; and integrated circuitry.
16 For instance, the invention encompasses a method of forming a capacitor
17 wherein a mass of silicon material is formed over a node location, and
18 wherein the mass comprises exposed doped silicon and exposed undoped
19 silicon. The method can further include substantially selectively forming
20 rugged polysilicon from the exposed undoped silicon and not from the
21 exposed doped silicon. Also, the method can include forming a capacitor
22 dielectric layer and a complementary capacitor plate proximate the rugged
23 polysilicon and doped silicon.

1 As another example, the invention encompasses a capacitor having a
2 capacitor dielectric layer intermediate a first capacitor plate and a second
3 capacitor plate, wherein at least one of the first and second capacitor plates
4 has a surface against the capacitor dielectric layer, and wherein said surface
5 comprises both doped rugged polysilicon and doped non-rugged polysilicon.

6 7 **BRIEF DESCRIPTION OF THE DRAWINGS**

8 Preferred embodiments of the invention are described below with
9 reference to the following accompanying drawings.

10 Fig. 1 is a schematic cross-sectional view of a semiconductor wafer
11 fragment comprising a prior art DRAM array.

12 Fig. 2 is a schematic cross-sectional process view of a semiconductor
13 wafer fragment at preliminary processing step of a processing method of the
14 present invention.

15 Fig. 3 is a view of the Fig. 2 wafer fragment at a processing step
16 subsequent to that of Fig. 2.

17 Fig. 4 is a view of the Fig. 2 wafer fragment at a processing step
18 subsequent to that of Fig. 3.

19 Fig. 5 is a view of the Fig. 2 wafer fragment at a processing step
20 subsequent to that of Fig. 4.

21 Fig. 6 is a view of the Fig. 2 wafer fragment at a processing step
22 subsequent to that of Fig. 5.

23 Fig. 7 is a view of the Fig. 2 wafer fragment at a processing step
24 subsequent to that of Fig. 6.

1 Fig. 8 is a view of the Fig. 2 wafer fragment at a processing step
2 subsequent to that of Fig. 7.

3 Fig. 9 is a top view of the Fig. 8 wafer fragment.

4 Fig. 10 is a view of the Fig. 2 wafer fragment at a processing step
5 subsequent to that of Fig. 8.

6 Fig. 11 is a view of the Fig. 2 wafer fragment at a processing step
7 subsequent to that of Fig. 10.

8 Fig. 12 is a view of the Fig. 2 wafer fragment at a processing step
9 subsequent to that of Fig. 11.

10 Fig. 13 is a view of the Fig. 2 wafer fragment at a processing step
11 subsequent to that of Fig. 12.

12 Fig. 14 is a view of the Fig. 2 wafer fragment at a processing step
13 subsequent to that of Fig. 6 processed according to a second embodiment of
14 the present invention.

15 Fig. 15 is a view of the Fig. 2 wafer fragment at a step subsequent
16 to that of Fig. 14.

17 Fig. 16 is a top view of the Fig. 15 wafer fragment.

18 Fig. 17 is a view of the Fig. 2 wafer fragment at a step subsequent
19 to that of Fig. 15.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Methods of forming DRAM arrays of the present invention are described with reference to Figs. 2-17, with Figs. 2-13 pertaining to a first embodiment of the invention, and Figs. 14-17 pertaining to a second embodiment of the invention. In describing the first embodiment of the present invention, like numerals from the preceding discussion of the prior art are utilized where appropriate, with differences being indicated by the suffix "a" or with different numerals.

Referring to Fig. 2, a semiconductor wafer fragment 10a is illustrated at a preliminary step of a process of the present invention. Wafer fragment 10a comprises a semiconductive material 12a, field oxide regions 14a, and a thin gate oxide layer 16a. Over gate oxide layer 16a is formed polysilicon layer 18a, silicide layer 20a and silicon oxide layer 22a. Silicide layer 20a comprises a refractory metal silicide, such as tungsten silicide, and polysilicon layer 18a typically comprises polysilicon doped with a conductivity enhancing dopant. Layers 16a, 18a, 20a and 22a can be formed by conventional methods.

Referring next to Fig. 3, polysilicon layer 18a, silicide layer 20a and silicon oxide layer 22a are etched to form wordlines 24a and 26a. Such etching can be accomplished by conventional methods. Between wordlines 24a and 26a are defined electrical node locations 25a, 27a and 29a, with

1 wordlines 26a comprising transistor gates which electrically connect node
2 locations 25a, 27a, and 29a. Node locations 25a, 27a and 29a are diffusion
3 regions formed within semiconductive material 12a.

4 Referring to Figs. 4 and 5, a nitride layer 28a is provided over
5 wordlines 24a and 26a and subsequently etched to form nitride spacers 30a
6 laterally adjacent wordlines 24a and 26a.

7 Referring to Fig. 6, an insulative material layer 34a is formed over
8 material 12a and over wordlines 24a and 26a. Insulative layer 34a may
9 comprise, for example, BPSG, and can be formed by conventional methods.
10 Insulative layer 34a comprises an upper surface 35a. Openings 38a, 39a and
11 40a are formed extending through insulative layer 34a to node locations 25a,
12 27a and 29a, respectively.

13 Referring to Fig. 7, an undoped silicon layer 100 is formed over
14 insulative layer 34a and within openings 38a, 39a and 40a. Undoped silicon
15 layer 100 narrows openings 38a, 39a and 40a, but does not fill such
16 openings. Undoped silicon layer 100 preferably has a thickness of from
17 about 50 Angstroms to about 1000 Angstroms, with a thickness of about 300
18 Angstroms being most preferred. Undoped silicon layer 100 preferably
19 comprises substantially amorphous silicon. Such substantially amorphous layer
20 can be 5-10% crystalline. Undoped silicon layer 100 can be formed by
21 conventional methods, such as, for example, by deposition utilizing either
22 silane or disilane. For purposes of the continuing discussion, and for
23 interpreting the claims that follow, "undoped" silicon is defined as silicon
24 having a dopant concentration of less than 5×10^{18} atoms/cm³, and "doped"

1 silicon is defined as silicon having a dopant concentration of at least
2 5×10^{18} atoms/cm³. "Undoped" silicon preferably comprises less than or
3 equal to 1×10^{18} atoms/cm³, and "doped" silicon preferably comprises at
4 least 1×10^{19} atoms/cm³.

5 A doped silicon layer 102 is formed over undoped silicon layer 100
6 and within openings 38a, 39a and 40a. In the shown embodiment of the
7 invention, doped layer 102 completely fills openings 38a, 39a and 40a.
8 However, in alternative embodiments of the invention, such as the embodiment
9 discussed below with reference to Figs. 14-17, layer 102 can only partially
10 fill openings 38a, 39a and 40a. As will be appreciated by persons of
11 ordinary skill in the art, the thickness of layer 102 will vary depending on
12 whether layer 102 is chosen to completely fill openings 38a, 39a and 40a,
13 or to partially fill such openings. Doped silicon layer 102 preferably
14 comprises doped polysilicon, and can be formed by conventional methods.

15 After formation of layers 100 and 102, an upper surface of wafer
16 fragment 10a is planarized to remove layers 100 and 102 from over insulative
17 layer 34a. Such planarization can be accomplished by, for example, chemical-
18 mechanical polishing (CMP).

19 Referring to Fig. 8, after the above-discussed planarization, pedestals
20 104, 106 and 108 remain in openings 38a, 39a and 40a (shown in Fig. 7),
21 respectively. Pedestals 104, 106 and 108 comprise undoped silicon layer 100
22 and doped silicon layer 102, and are over node locations 25a, 27a and 29a,
23 respectively. Pedestals 104, 106 and 108 also comprise exposed upper
24 surfaces 116, 118 and 120, respectively.

1 Fig. 9 illustrates a top view of the Fig. 8 wafer fragment, and shows
2 that pedestals 104, 106 and 108 actually comprise a core of doped silicon
3 layer 102 surrounded by undoped silicon layer 100.

4 Referring again to Fig. 8, insulative layer 34a is selectively removed
5 relative to the silicon of pedestals 104, 106 and 108 to form a new upper
6 surface 37a lower than previous upper surface 35a (shown in Fig. 7). The
7 preferred BPSG insulative layer 34a can be selectively removed relative to
8 pedestals 104, 106 and 108 using a conventional oxide etch. The selective
9 removal of insulative layer 34a exposes a sidewall surface 110 of pedestal
10 104, a sidewall surface 112 of pedestal 106, and a sidewall surface 114 of
11 pedestal 108. Sidewall surfaces 110, 112 and 114 comprise undoped silicon
12 layer 100. Additionally, in the shown embodiment a portion of undoped
13 silicon layer 100 is below upper surface 37a of BPSG layer 34a, and remains
14 unexposed. The depth of removal of insulative layer 34a can be controlled
15 by a number of methods. For example, layer 34a could be removed via a
16 timed etch. As another example, an etch stop layer could be formed within
17 layer 34a at a desired depth of surface 37a. An example of a layer 34a
18 comprising an etch stop layer is a layer comprising BPSG and having a
19 silicon nitride etch stop layer formed within the BPSG at a level of upper
20 surface 37a.

21 As exposed sidewall surfaces 110, 112 and 114 of pedestals 104, 106
22 and 108 comprise undoped silicon layer 100, and as exposed upper surfaces
23 116, 118 and 120 of the pedestals comprise exposed doped silicon layer 102,
24 as well as exposed undoped silicon layer 100, the pedestals comprise exposed

1 doped silicon and exposed undoped silicon at the processing step of Fig. 8.

2
3 Referring to Fig. 10, a rugged polysilicon layer 122 is substantially
4 selectively formed from the exposed undoped silicon of surfaces 110, 112 114,
5 116, 118, and 120 (shown in Fig. 8), and not from the exposed doped
6 silicon of surfaces 116, 118 and 120. Rugged polysilicon layer 122
7 comprises materials selected from the group consisting of HSG and cylindrical
8 grain polysilicon. The substantially selective formation of a preferred HSG
9 polysilicon layer 122 from undoped silicon surfaces but not from doped
10 silicon surfaces can be accomplished by the following process.

11 First, wafer fragment 10a is loaded into a conventional chemical vapor
12 deposition (CVD) furnace and is subjected to an *in situ* hydrofluoric acid
13 (HF) clean to remove native oxide. The *in situ* HF clean preferably
14 comprises a flow rate of 85 standard cubic centimeters per minute (sccm) of
15 HF gas and 8500 sccm of H₂O gas, at a pressure of 15 Torr, for a time
16 of about 20 seconds. Wafer fragment 10a is then exposed to silane to form
17 amorphous silicon seeds on the undoped silicon. Wafer fragment 10a is then
18 annealed for approximately 20 minutes at about 560°C. The seeding and
19 anneal steps convert undoped amorphous silicon into rugged polysilicon (such
20 as hemispherical grain polysilicon), while leaving exposed doped silicon layers
21 not converted to rugged polysilicon. It is noted that the above-described
22 process for forming HSG polysilicon does not require disilane, and hence is
23 different than the "pure" selective hemispherical grain deposition utilized in
24 high vacuum tools with disilane.

1 After the formation of rugged polysilicon layer 122, a short polysilicon
2 etch is performed to remove any monolayers of silicon deposited on insulative
3 layer 34a during the above-described seeding step. Such polysilicon etch can
4 be accomplished with conventional conditions, and may comprise either a wet
5 etch or a dry etch.

6 The above-described process for forming rugged polysilicon layer 122
7 advantageously avoids formation of polysilicon on a back side (not shown) of
8 wafer fragment 10a. The method can also avoid double bit failures by
9 removing monolayers of silicon after formation of HSG.

10 Subsequent thermal processing of pedestals 104, 106 and 108 can out-
11 diffuse dopant from doped polysilicon layer 102 into undoped silicon layer
12 100 (shown in Fig. 8), to convert unexposed portions of undoped silicon layer
13 100 into a doped polysilicon layer 119. Subsequent thermal processing can
14 also out-diffuse dopant from doped polysilicon layer 102 into rugged
15 polysilicon layer 122. Thermal processing to out-diffuse dopant from doped
16 polysilicon layer 102 into adjacent undoped layers will typically comprise
17 temperatures of 800° C or greater.

18 Referring to Fig. 11, a dielectric layer 124 is provided over insulative
19 layer 34a and over pedestals 104, 106 and 108. Dielectric layer 124 will
20 typically comprise silicon nitride and/or silicon oxide, although other suitable
21 materials are known to persons of skill in the art. A capacitor cell plate
22 layer 126 is provided over dielectric layer 124. Capacitor cell plate layer
23 126 will typically comprise doped polysilicon, but other suitable materials are
24 known to persons of skill in the art.

1 Referring to Fig. 12, a patterned masking layer 128 is formed over
2 pedestals 104 and 108, leaving pedestal 106 exposed. Subsequently, wafer
3 fragment 10a is subjected to etching conditions which remove cell plate layer
4 126 and dielectric layer 124 from proximate pedestal 106. After such
5 etching, pedestal 106 is electrically isolated from pedestals 104 and 108, with
6 the only remaining electrical connection between pedestal 106 and pedestals
7 104 and 108 being through wordlines 26a. Methods for removing cell plate
8 layer 126 and dielectric layer 124 from proximate pedestal 106 are known to
9 persons of ordinary skill in the art.

10 Referring to Fig. 13, masking layer 128 is removed and an insulative
11 layer 130 is formed over pedestals 104, 106 and 108, and over insulative
12 layer 34a. Insulative layer 130 may comprise, for example, BPSG, and can
13 be formed by conventional methods. A conductive bitline plug 75a is formed
14 extending through insulative layer 130 and in electrical contact with pedestal
15 106. Pedestal 106 comprises rugged lateral surfaces 136 and an upper surface
16 118 which has a predominant portion not comprising rugged-polysilicon. As
17 shown, the non-rugged polysilicon of upper surface advantageously provides a
18 smooth landing region for bitline plug 75a.

19 Pedestal 106 and bitline plug 75a together form a bitline contact 77a.
20 A bitline 76a is formed over bitline plug 75a and in an electrical connection
21 with pedestal 106 through bitline plug 75a. Bitline 76a and bitline plug 75a
22 may be formed by conventional methods.
23
24

1 The above-describe method can be used to avoid chemical-mechanical
2 polishing of a rugged polysilicon layer, thus avoiding a potential source of
3 double bit failures.

4 Fig. 13 illustrates a DRAM array 83a of the present invention. DRAM
5 array 83a comprises capacitors 62a and 64a. Capacitors 62a and 64a
6 comprise capacitor storage nodes 132 and 134, respectively, which comprise
7 doped polysilicon layer 102, doped polysilicon layer 119 and rugged-polysilicon
8 layer 122. As the doped polysilicon layer 119 is formed from the undoped
9 silicon layer 100 (shown in Fig. 8), the undoped silicon layer 100 and doped
10 silicon layer 102 of pedestals 104 and 108 in Fig. 8 together define capacitor
11 storage nodes 132 and 134. Storage nodes 132 and 134 have rugged-
12 polysilicon-comprising lateral surfaces 138 and 140, respectively. Storage
13 nodes 132 and 134 further comprise top surfaces 116 and 120, respectively,
14 which have predominant portions which do not comprise rugged-polysilicon.

15 Cell plate layer 126 and dielectric layer 124 are operatively proximate
16 to storage nodes 132 and 134 so that the storage nodes, together with cell
17 plate layer 126 and dielectric layer 124, form operative capacitors 62a and
18 64a. Dielectric layer 124 contacts rugged surfaces 138 and 140, as well as
19 top surfaces 116 and 120 of storage nodes 132 and 134.

20 Capacitors 62a and 64a are connected to pedestal 106 through wordlines
21 26a. Capacitor 62a, together with bitline contact 77a and an interconnecting
22 wordline 26a, comprises a first DRAM cell 79a. Capacitor 64a, together with
23 bitline contact 77a and an interconnecting wordline 26a, comprises a second
24 DRAM cell 81a.

1 A second embodiment of the invention is described with reference to
2 Figs. 14-17. In describing the embodiment of Figs. 14-17, numbering similar
3 to that utilized above for describing the embodiment of Figs. 2-13 is utilized,
4 with differences being indicated by the suffix "b", or by different numbers.

5
6 Referring to Fig. 14, a wafer fragment 10b is shown at a processing
7 step subsequent to that of the above-discussed Fig. 6. Wafer fragment 10b
8 comprises wordlines 24b and 26b having constructions identical to that
9 discussed above with regard to the prior art. Wafer fragment 10b further
10 comprises node locations 25b, 27b and 29b between wordlines 24b and 26b.
11 Wafer fragment 10b also comprises a semiconductor substrate 12b and field
12 oxide regions 14b formed over substrate 12b.

13 An insulative material layer 34b is formed over wordlines 24b and 26b,
14 and over semiconductive material 12b. Insulative layer 34b may comprise a
15 number of materials known to persons of ordinary skill in the art, including
16 BPSG. Openings 38b, 39b and 40b extend through insulative layer 34b to
17 node locations 25b, 27b and 29b, respectively.

18 A first undoped silicon layer 146 extends over insulative layer 34b and
19 within openings 38b, 39b and 40b. Undoped silicon layer 146 preferably
20 comprises amorphous silicon, and preferably has a thickness of from about 50
21 Angstroms to about 500 Angstroms. Undoped silicon layer 146 can be
22 formed by conventional methods, such as CVD. Undoped silicon layer 146
23 narrows openings 38b, 39b and 40b.
24

9 A second undoped silicon layer 150 is formed over doped silicon
10 layer 148 and within openings 38b, 39b and 40b. Undoped silicon layer 150
11 preferably comprises the same preferable materials of first undoped silicon
12 layer 146. Accordingly, second undoped silicon layer 150 preferably
13 comprises substantially amorphous silicon. Second undoped silicon layer 150
14 preferably has a thickness of from 50 to 500 Angstroms, and in the shown
15 preferred embodiment does not fill openings 38b, 39b and 40b.

After formation of layers 146, 148 and 150, wafer fragment 10b is planarized to remove layers 146, 148 and 150 from over insulative layer 34b. Such planarizing may be accomplished by, for example, chemical-mechanical polishing. After the planarization of wafer fragment 10b, pedestals 104b, 106b and 108b (shown in Fig. 15) having upper surfaces 116b, 118b and 120b (shown in Fig. 15), respectively, remain within openings 38b, 39b and 40b.

Referring to Fig. 15, the material of insulative layer 34b is selectively removed relative to the silicon of pedestals 104b, 106b and 108b to form an

1 upper surface 37b of insulative layer 34b which is below upper surfaces 116b,
2 118b and 120b of pedestals 104b, 106b and 108b. The removal of insulative
3 layer 34b exposes sidewalls 110b, 112b and 114b of pedestals 104b, 106b and
4 108b, respectively. The exposed sidewalls 110b, 112b and 114b comprise first
5 undoped silicon layer 146. Additionally, in the shown embodiment a portion
6 of undoped silicon layer 146 is below upper surface 37b of BPSG layer 34b,
7 and remains unexposed. In the shown preferred embodiment, pedestals 104b,
8 106b and 108b comprise hollow interiors corresponding to openings 38b, 39b
9 and 40b (shown in Fig. 14). The depth of removal of insulative layer 34b
10 can be controlled by methods such as those discussed above with reference
11 to Fig. 8 for controlling the depth of removal of insulative layer 34a.

12 Referring to Fig. 16, which is a top view of the Fig. 15 wafer
13 fragment, second undoped silicon layer 150 lines the hollow interiors
14 corresponding to openings 38b, 39b and 40b.

15 Referring to Fig. 17, wafer fragment 10b is subjected to processing
16 identical to that discussed above regarding Fig. 10 to convert exposed undoped
17 silicon surfaces to rugged-polysilicon surfaces, while not roughening exposed
18 doped silicon surfaces. Such treatment forms a rugged-polysilicon layer 122b
19 from exposed portions of first undoped silicon layer 146 (shown in Fig. 15)
20 and forms a rugged-polysilicon layer 160 from second undoped silicon layer
21 150 within the interiors of pedestals 104b, 106b and 108b. Such processing
22 also out-diffuses dopant from doped silicon layer 148 into adjacent undoped
23 layers and thus converts unexposed portions of undoped layer 146 (shown in
24 Fig. 15) into doped regions 119b.

1 Subsequent processing, similar to the processing discussed above with
2 reference to Figs. 11-13, may be conducted to form a DRAM array from
3 pedestals 104b, 106b and 108b. In such DRAM array, pedestals 104b and
4 108b would be storage nodes for first and second capacitors, respectively, and
5 pedestal 106b would form a conductive contact to a bitline. Such subsequent
6 processing is not illustrated as the description above regarding Figs. 11-13 is
7 sufficient to enable a person of skill in the art to form a DRAM array from
8 the structure of Fig. 17. It is noted, however, that the storage nodes formed
9 from pedestals 104b and 108b would differ from the storage nodes of Fig. 13
10 in that the storage nodes formed from pedestals 104b and 108b would have
11 the shape of upwardly open containers, with the interiors of such containers
12 being lined by rugged-polysilicon layer 160.

13 The above-described DRAMs and capacitors of the present invention can
14 be implemented into monolithic integrated circuitry, including microprocessors.

15
16 To aid in interpretation of the claims that follow, the term
17 "semiconductive substrate" is defined to mean any construction comprising
18 semiconductive material, including, but not limited to, bulk semiconductive
19 materials such as a semiconductive wafer (either alone or in assemblies
20 comprising other materials thereon), and semiconductive material layers (either
21 alone or in assemblies comprising other materials). The term "substrate"
22 refers to any supporting structure, including, but not limited to, the
23 semiconductive substrates described above.
24

